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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,798	12/11/2006	Bernard Aspar	288918US6PCT	2578

22850 7590 09/24/2010
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1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER

SLUTSKER, JULIA

ART UNIT	PAPER NUMBER
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2891

NOTIFICATION DATE	DELIVERY MODE
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09/24/2010

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/574,798	Applicant(s) ASPAR ET AL.	
	Examiner JULIA SLUTSKER	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 38-98 is/are pending in the application.
- 4a) Of the above claim(s) 38-67, 80-84 and 97 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 68-79, 85-96, and 98 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 July 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>07/15/2010</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 68, 73-75, 78, 85, and 87-93 are rejected under 35 U.S.C. 102(e) as being anticipated by MacNamara (US 6, 841, 848).

Regarding claim 68, MacNamara discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig.4, numeral 9) including a transplant layer (upper part of (9)) that has at least one of circuit and components (note: since (9) is a device wafer, it has at least one of circuit and components), comprising: eliminating material from the first wafer (Fig.8, numeral 9; column 9, lines 30-45), having the transplant layer (Fig.8, upper part of numeral 9) from a frontal side of the first wafer (9), the transplant layer arranged at least under the frontal side of the first wafer (Fig.8 upper part of (9)), over a thickness less than a thickness of the first wafer, (Fig.8, numeral 9) but greater than a thickness of the transplant layer (Fig.8, upper part of numeral 9); and

Art Unit: 2891

assembling the transplant layer (Fig.10, lower part of numeral 9) onto a second wafer or material (Fig.10, numeral 30).

Regarding claim 73, MacNamara discloses that a part of the material of the transplant layer is eliminated during the eliminating (Fig.8, numeral 25).

Regarding claim 74, MacNamara discloses that the first wafer is chamfered and includes at least a chamfered edge (Fig.7, numeral 26).

Regarding claim 75, MacNamara discloses that the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane (Fig.8, numeral W).

Regarding claim 78, MacNamara discloses that the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of a zone of the first wafer which can not, without eliminating, be assembled with the second wafer (Fig.8, numeral W).

Regarding claim 85, MacNamara discloses that the assembling the first and second wafers is performed via molecular bonding (column 9, lines 50-67).

Regarding claim 87, MacNamara discloses that the eliminating takes place after a previous surface preparation of the first wafer for a purpose of assembling (column 9, lines 15-20).

Regarding claim 88, MacNamara discloses the eliminating takes place before a previous surface penetration of the first wafer for a purpose of assembling or transplanting (column 9, lines 50-55).

Regarding claim 89, MacNamara discloses that the routing is performed via plasma etching (column 9, lines 25-50).

Regarding claim 90, MacNamara discloses that at least one of the first and second wafers is made in a semiconductor material (column 8, lines 1-15).

Regarding claim 91, MacNamara discloses at least one of the first and second wafers is made of silicon (column 8, lines 1-15).

Regarding claim 92, MacNamara discloses at least one of the first and second wafers is made of an insulating material (column 8, lines 1-15).

Regarding claim 93, MacNamara discloses that the eliminating is performed in a regular manner around the first wafer (Fig.8).

3. Claims 68, 76, 86, 94-96, and 98 rejected under 35 U.S.C. 102(b) as being anticipated by Oi (US 2003/0092244).

Regarding claim 68, Oi discloses a method of assembling a first wafer onto a second wafer, the first wafer including a transplant layer (Fig.2B, upper part of (10) note: since the upper part of (10) is transplanted to (20) in Fig. 3K, it is considered as a transplant layer) that has components (11), comprising: eliminating material from the first wafer of material (Fig.1, numeral 13) having the transplant layer is made (Fig.2d, upper part of (10)), from a frontal side of the first wafer (1), the transplant layer arranged at least under the frontal side of the wafer (Fig.2b, upper part of (10) over a thickness less than a thickness of the first wafer (Fig.2d, numeral 10), but greater than a thickness of the transplant layer (Fig.2d, upper part of (10))); and assembling the transplant layer of the first wafer onto a second wafer or material (Fig.3K).

Regarding claim 76, Oi discloses an eliminating of material after assembling the first and second wafers (Fig.3j).

Regarding claim 86, Oi discloses that components of the transplant layer are made in the first wafer before the eliminating (Fig.2b, numeral 11).

Regarding claim 94, Oi discloses that the eliminating is performed in an irregular manner around the first wafer, creating a plane (Fig.2c, numeral 13).

Regarding claim 95, Oi discloses that the eliminating is performed in an irregular manner, creating a marking zone (Fig.2c, numeral 13).

Regarding claim 96, Oi discloses marking the first wafer (Fig.2c, numeral 13).

Regarding claim 98, Oi discloses additional eliminating of material of the first wafer from a lateral side of the first wafer over a length l_2 that removes some material of the transplant layer (Fig.3j).

4. Claim 68, 74, 76, 77, and 98 are rejected under 35 U.S.C. 102(b) as being unpatentable over Iyer (US 5, 937, 312).

Regarding claim 68, Iyer discloses a method of assembling a first wafer onto a second wafer, the first wafer (Fig. 1, numeral 20) including a transplant layer (Fig.1, numeral 22) that has at least one of circuits and components (note: since (22) is a device layer, it has at least one of circuits and components), comprising: eliminating material from the first wafer (Fig.4, numeral 34), having the transplant layer (22) from a frontal side of the first wafer (32), the transplant layer (22) arranged at least under the frontal side of the first wafer (32), over a thickness less than a thickness of the first wafer (30), but greater than a thickness of the transplant layer (22) (note: (22) is 0.5-

Art Unit: 2891

50 μ m, (20) is 300-800 μ m and after eliminating the wafer (20) is 20-35 μ m) ; and assembling the transplant layer (Fig.4, numeral 22) of the first wafer (Fig.4, numeral 20) onto a second wafer (Fig.4, numeral 26).

Regarding claim 74, Iyer discloses that the first wafer is chambered and includes at least a chamfered edge (Fig.3, numeral 20).

Regarding claim 76, Iyer discloses additional eliminating of material after said assembling of the first and second wafer (Fig.6).

Regarding claim 77, Iyer discloses that eliminating is performed over a thickness of the first wafer between 1 mm and 100 mm (column 4, lines 56-50).

Regarding claim 98, Iyer discloses additional eliminating of material from the first wafer from a lateral side of the first wafer of a length L_2 that removes some material of the transplant layer (Fig.6)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 77 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacNamara.

Regarding claim 77, MacNamara does not disclose the eliminating is performed over a thickness of the first wafer between 1 μ m and 100 μ m.

MacNamara however discloses that eliminating is performed to avoid danger of an unbounded peripheral area being formed around of a composite wafer (column 8, lines 53-60).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the lamination process (MacNamara, column 8, lines 53-60).

Regarding claim 79, MacNamara does not disclose that the eliminating is performed over a width, measured on a plane parallel to that of the first wafer of between 100 μm and 5 μm .

MacNamara however discloses that eliminating is performed to avoid danger of an unbounded peripheral area being formed around of a composite wafer (column 8, lines 53-60).

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first wafer to be in the claimed range for the purpose of optimizing the lamination process (MacNamara, column 8, lines 53-60).

7. Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer as applied to claim 68 above, and further in view of Sakaguchi (US 2002/0068419).

Regarding claim 86, Iyer does not disclose that components or circuits are made in the first wafer before routing.

Iwasaki however discloses that the device layer is formed in the first wafer (Fig.1, numeral 22). And Sakaguchi discloses that circuits are formed in the semiconductor layer in advance ([0095]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Iyer with Sakaguchi to made circuits in the first wafer before eliminating for the purpose of conveniently forming a semiconductor device (Sakaguchi, [0002]).

Response to Arguments

8. Applicant's arguments filed 07/15/2010 have been fully considered but they are not persuasive.

9. The applicant's arguments that MacNamara does not disclose eliminating material from the first wafer greater than the thickness of the transplant layer are not persuasive, since the device layer (2) (i.e. the transplant layer) which is formed from the upper portion of (9) is mechanically grinded to the thickness, t (Fig.11, column 10, lines 5-15). Thus, the eliminating material from the first wafer (9) in Fig.8 is greater than the thickness of the transplant layer (2) in Fig.11.

10. The applicant's arguments that Oi does not disclose eliminating material from the first wafer greater than the thickness of the transplant layer are not persuasive, since the transplant layer of Oi (Fig.3K, numeral 10A) which is formed from the upper portion of (10) is grounded ([0011]), i.e. the eliminating material from the first wafer performed in Fig.2C (numeral 13) is greater than the thickness of the transplant layer (10A) in Fig.3K.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2891

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

September 15, 2010

/Asok K. Sarkar/

Primary Examiner, Art Unit 2891

September 20, 2010